REMARKS

The Examiner has rejected Claims 1-14, and 21 under 35 U.S.C. 101 as being directed towards non-statutory subject matter. Applicant has amended independent Claims 1, 9, and 21 in order to avoid such rejection.

The Examiner has rejected Claim 8 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, the Examiner has argued that Claim 8 "recites the limitation 'linked-list data structures' in line 4" and that "there is insufficient antecedent basis for this limitation in the claim." Applicant respectfully asserts that such rejection has been avoided in view of the amendments made to Claim 1.

The Examiner has rejected Claims 1 and 3-7 under 35 U.S.C. 102(b) as being anticipated by Harriman et al. (U.S. Patent No. 5,898,687). Applicant respectfully disagrees with such rejections, especially in view of the amendments made hereinabove to the independent claims. Specifically, applicant has amended independent Claim 1 to at least substantially include the subject matter of former dependent Claim 2.

With respect to independent Claim 1, the Examiner has relied on item 128 of Figure 1; item 300 of Figure 3; Col.4, lines 38-39; and Col. 7, line 8 from the Harriman reference to make a prior art showing of applicant's claimed technique "wherein the packet controller is configured to receive a first sequence of packet pointers and to provide each packet pointer to one of the first and second data structures."

Applicant respectfully asserts that item 128 of Figure 1 from Harriman merely shows an address pointer, where "[u]pon receiving a cell from the source port 102, the switching fabric 110 extracts the payload data from the cell, stores it in its shared memory 112 over line 115 and records the memory address of that payload location in an address pointer 128" (Col. 4, lines 34-38 - emphasis added). Additionally, in Col.4, lines 38-39, Harriman merely teaches that "[t]he payload location recorded in the pointer 128 comprises a K-bit memory address" (emphasis added). However, simply disclosing that

"the switching fabric...records the memory address of that payload location in an address pointer 128" where "the pointer 128 comprises a K-bit memory address" (emphasis added), as in Harriman, fails to teach that "the packet controller is configured to receive a first sequence of packet pointers" (emphasis added), as claimed by applicant.

Furthermore, applicant respectfully asserts that item 300 of Figure 3, and Col. 7, line 8 from Harriman merely disclose a "fair-sharing arbitration policy 300." However, merely disclosing a "fair-sharing arbitration policy" (emphasis added), as in Harriman, fails to even suggest that "the packet controller is configured to...provide each packet pointer to one of the first and second data structures" (emphasis added), as claimed by applicant. Moreover, the excerpts and figures from Harriman relied upon by the Examiner fail to teach or even suggest that "the packet controller is configured to receive a first sequence of packet pointers **and** to provide each packet pointer to one of the first and second data structures" (emphasis added), as claimed by applicant.

Additionally, with respect to independent Claim 1, the Examiner has relied on item 320 of Figure 3; Col. 7, lines 20-23; and Col. 7, lines 32-33 from the Harriman reference to make a prior art showing of applicant's claimed "port transmit controller coupled to the first and second data structures and configured to provide a second sequence of packet pointers."

Applicant respectfully asserts that item 320 of Figure 3 from Harriman merely shows a strict priority (SP) component. Further, the excerpts from Harriman relied upon by the Examiner merely teach that "priority [is] determined by, inter alia, the queue occupancy calculation" and that "the queue service algorithm at the output ports is strict priority (SP) as indicated by the SP component 320" (Col. 7, lines 20-23). However, simply teaching that "priority [is] determined by...the queue occupancy calculation" where "the queue service algorithm at the output ports is strict priority" (emphasis added), as in Harriman, simply fails to teach "a port transmit controller...configured to provide a second sequence of packet pointers" (emphasis added), as claimed by applicant.

The Examiner is reminded that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, the identical invention must be shown in as complete detail as contained in the claim. *Richardson v. Suzuki Motor Co.*868 F.2d 1226, 1236, 9USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim.

This criterion has simply not been met by the excerpt(s) from the above reference, as noted above. Nevertheless, despite such paramount deficiencies and in the spirit of expediting the prosecution of the present application, applicant has incorporated the subject matter of former Claim 2 into independent Claim 1.

The Examiner has rejected Claims 9-12 and 14-31 under 35 U.S.C. 103(a) as being unpatentable over Harriman et al., in view of Raza et al. (U.S. Patent No. 7,016,349). Applicant respectfully disagrees with such rejections, especially in view of the amendments made hereinabove to the independent claims. Specifically, applicant has amended each of the independent claims to at least substantially include the subject matter of former dependent Claim 2.

With respect to independent Claim 9, the Examiner has relied on item 108 of Figure 6 and Col. 7, lines 48-50 and 52 from Raza to make a prior art showing of applicant's claimed "third data structure...coupled to the second data structure and configured to store a plurality of status flags."

Applicant respectfully asserts that item 108 of Figure 6 from Raza merely shows a logic block, where "[t]he write interface 104' may communicate with the logic block 108' by presenting/receiving a signal (e.g., WR_CTRL) to determine an address for storing the incoming data and status of the flags for a particular queue" (Col. 7, lines 45-49 – emphasis added). Furthermore, in Col. 7, lines 49-52, Raza merely teaches that "[t]he write interface 104' may then write the data into the dual port memory 102'"and

"[t]he read interface 106' may receive a read address and flag status of the FIFOs from the logic block 108' (via the signal RD_CTRL)" (emphasis added).

However, merely disclosing "[t]he read interface 106' may receive a read address and flag status of the FIFOs from the logic block 108'" (emphasis added), as in Raza, fails to even suggest "a third data structure...coupled to the second data structure and configured to store a plurality of status flags" (emphasis added), as claimed by applicant.

With respect to independent Claim 15, the Examiner has relied on item 132 of Figure 1 and Col. 4, lines 41-43 from Harriman to make a prior art showing of applicant's claimed "if the pointer is the first type, determining if an overall tail is the first type or the second type" and "if the pointer is the second type, determining if the overall tail is the first type or the second type."

Applicant respectfully asserts that item 132 of Figure 1 from Harriman merely shows "a key over line." Furthermore, in Col. 4, lines 40-43, Harriman merely teaches that "[t]he ITF 120 processes the remaining header information to generate ... a key over line 132 indicating whether the cell requires multicast replication" (emphasis added).

However, merely teaching that "[t]he ITF 120 processes the remaining header information to generate ... a key over line 132 indicating whether the cell requires multicast replication" (emphasis added), as in Harriman, simply fails to teach that "if the pointer is the first type, determining if an overall tail is the first type or the second type" or "if the pointer is the second type, determining if the overall tail is the first type or the second type" (emphasis added), as claimed by applicant. Clearly, "indicating whether the cell requires multicast replication" (emphasis added), as in Harriman, simply fails to teach "determining if an overall tail is the first type or the second type" (emphasis added), as claimed by applicant.

Additionally, with respect to independent Claim 15, the Examiner has relied on the system 400 from Figure 13 and Col. 14, lines 27-29 from Raza to make a prior art showing of applicant's claimed "if the overall tail is the second type, setting an overall

tail flag to a first state, and setting an entry to the first state" and "if the overall tail is the first type, adding the pointer to the second data structure field with the first state."

Applicant respectfully asserts that, in Col. 14, lines 27-29, Raza merely teaches that "the system 400 may allow a multicast queue to send a single location and unicast queue to implement complex processing" (emphasis added). However, simply disclosing that "the system 400 may allow a multicast queue to send a single location and unicast queue to implement complex processing" (emphasis added), as in Raza, fails to even suggest, "if the overall tail is the second type, **setting** an overall tail flag to a first state, and setting an entry to the first state" (emphasis added), as claimed by applicant.

Further, disclosing that "the system 400 may allow a multicast queue to send a single location and unicast queue to implement complex processing" (emphasis added), as in Raza, fails to even suggest, "if the overall tail is the first type, adding the pointer to the second data structure field with the first state" (emphasis added), as claimed by applicant.

Still yet, with respect to independent Claim 15, the Examiner has relied on the system 400 from Figure 13 and Col. 14, lines 23-25 from Raza to make a prior art showing of applicant's claimed "if the overall tail is the second type, adding the pointer to a second data structure field with a second state."

Applicant respectfully asserts that, in Col. 14, lines 23-25, Raza merely teaches that "[t]he system 400 compris[es] a multicast pointer logic block configured to generate and store multicast addresses" (emphasis added). However, simply disclosing that "[t]he system 400 compris[es] a multicast pointer logic block configured to generate and store multicast addresses" (emphasis added), as in Raza, simply fails to teach "if the pointer is the second type and the overall tail is the second type, adding the pointer to the second data structure field with a second state" (emphasis added), as claimed by applicant.

Additionally, with respect to independent Claim 15, the Examiner has relied on the Col. 15, lines 2-3 from Raza to make a prior art showing of applicant's claimed

"setting the first type tail to the pointer" and "setting the overall tail flag to the second state."

Applicant respectfully asserts that the excerpt from Raza relied upon by the Examiner simply teaches "the configuration logic 502 writes to the queue pointer memory 504." However, simply teaching that "the configuration logic 502 writes to the queue pointer memory 504" (emphasis added), as in Raza, fails to teach or even suggest "setting the first type tail to the pointer" (emphasis added) or "setting the overall tail flag to the second state" (emphasis added), as claimed by the applicant. Clearly, writing to "the queue pointer memory" (emphasis added), as in Raza, simply fails to suggest "setting the first type tail to the pointer" (emphasis added) or "setting the overall tail flag to the second state" (emphasis added), as claimed by the applicant.

Further, with respect to independent Claim 15, the Examiner has relied on the following excerpts from Raza to make a prior art showing of applicant's claimed "getting a first type tail" and "linking the pointer in a first data structure to the first type tail."

> "When writing data to a different queue, the write pointer (or tail pointer) may be fetched from the FIFO pointer memory 134 (also called the queue pointer memory)." (Col. 7, lines 9-12)
>
> "When a new queue address is requested for a read or write operation, the address logic block 130 generally requests the data from the pointer memory 134." (Col. 7, lines 29-32)

Applicant respectfully asserts that the excerpts from Raza relied upon by the Examiner simply teach that "[w]hen writing data to a different queue, the write pointer (or tail pointer) may be fetched from the FIFO pointer memory" (emphasis added). However, merely teaching that the "tail pointer ... may be fetched from the FIFO pointer memory" (emphasis added), as in Raza, fails to disclose "getting a first type tail" (emphasis added), as claimed by applicant. More specifically, Raza fails to teach "getting a first type tail," where the "overall tail is the second type" (emphasis added), as in the context claimed by applicant (see Claim 15 for context).

Furthermore, in Col. 7, lines 29-32, Raza simply teaches that "[w]hen a new queue address is requested for a read or write operation, the address logic block 130 generally requests the data from the pointer memory 134" (emphasis added). However, simply teaching that the "address logic block 130 ... requests ... data from pointer memory 134" (emphasis added) when a new queue address is requested, as in Raza, simply fails to disclose "linking the pointer in a first data structure to the first type tail" (emphasis added), as claimed by applicant. More specifically, Raza fails to teach "linking the pointer in a first data structure to the first type tail" (emphasis added) where the "overall tail is the second type" (emphasis added), as in the context claimed by applicant (see Claim 15 for context).

With respect to independent Claim 21, it appears the Examiner has failed to rely on any specific citations from the prior art in the rejection of such claim. Because Claim 21 recites similar limitations to Claim 15, Claim 21 is also believed to be allowable over the prior art of record.

With respect to independent Claims 22 and 28, the Examiner has relied on Col. 18, lines 63-64 from Raza to make a prior art showing of applicant's claimed "if the overall head is the first type... updating the first type head with a next pointer from a first data structure."

Applicant respectfully asserts that, in Col. 18, lines 59-64, Raza merely teaches that "[w]hen a contention occurs, the data (e.g., the signal WRITE_DATA_DP) from a write register (e.g., a register block 954 to be discussed in connection with FIG. 20) may be directly passed (through the multiplexer 908) to the output of the circuit 900 while the data is being written into the dual-port memory 906." However, simply disclosing that "data...from a write register...may be directly passed...to the output of the circuit 900 while the data is being written into the dual-port memory," as in Raza, fails to even suggest "if the overall head is the first type... updating the first type head with a next pointer from a first data structure" (emphasis added), as claimed by applicant.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the excerpts from the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above. Nevertheless, despite such paramount deficiencies and in the spirit of expediting the prosecution of the present application, applicant has incorporated the subject matter of former Claims 2 et al. into the independent claims.

With respect to the subject matter of former Claim 2 (now at least substantially incorporated into the independent claims), the Examiner has rejected the same under 35 U.S.C. 103(a) as being unpatentable over Harriman. Specifically, the Examiner has argued that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to modify Harriman et al.'687's system to incorporate that the first data structure includes a plurality of linked-list data structures." In addition, the Examiner has argued that "[t]he motivation to combine these teachings is to increase the replication rate of a switching fabric circuit having a multicasting capability that requires minimal buffer capacity for multicast connection traffic (column 1, lines 60-64)."

Applicant respectfully disagrees and asserts that, in Col. 1, lines 60-64, Harriman merely teaches that "[t]he invention is directed to a mechanism for increasing the replication rate of a switching fabric circuit having a multicasting capability that requires minimal buffer capacity for multicast connection traffic."

However, merely disclosing "a mechanism for increasing the replication rate of a switching fabric circuit having multicasting capability that requires minimal buffer capacity for multicast connection traffic" (emphasis added), as in Harriman, does not even suggest "[a] first data structure includ[ing] a plurality of linked-list data structures" (emphasis added), as claimed by applicant (see this or similar, but not necessarily identical language in the independent claims).

Because Harriman fails to teach or suggest "[a] first data structure includ[ing] a plurality of linked-list data structures" (emphasis added), as claimed by applicant, it cannot be said that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to modify Harriman et al.'687's system to incorporate that the first data structure includes a plurality of linked-list data structures," as argued by the Examiner. Applicant thus formally requests a specific showing of the subject matter in ALL of the claims in any future action.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to dependent Claim 8, the Examiner has rejected the same under 35 U.S.C. 103(a) as being unpatentable over Harriman. Specifically, the Examiner has relied on Col. 7, lines 13-14 and Col. 2, lines 38-41 from Harriman to make a prior art showing of applicant's claimed technique "wherein...the packet controller is configured to provide ... each of the plurality of second type packet pointers to each or a group of the plurality of FIFO structures."

Applicant respectfully asserts that the excerpts relied upon by the Examiner simply teach that "each port of the switch has a unicast/multicast output queue pair for each predetermined priority level" (Col. 7, lines 13-15 – emphasis added) and that "there is preferably one multicast output queue for each output port of the switch at each predetermined priority level" (Col. 2, lines 39-41 – emphasis added). However, merely teaching that "each port of the switch has a unicast/multicast output queue pair for each predetermined priority level" (emphasis added) and that "there is preferably one multicast output queue for each output port of the switch at each predetermined priority level" (emphasis added), as in Harriman, fails to disclose "the packet controller is configured to

provide ... each of the plurality of second type packet pointers to each or a group of the plurality of FIFO structures" (emphasis added), as claimed by applicant.

In addition, with respect to Claim 8, the Examiner has stated that "Harriman et al. '687 does not teach that the packet controller is configured to provide each of the plurality of first type packet pointers to a selected one of the plurality of linked-list data structures" but argues that "providing each of the plurality of first type packet pointers to a selected one of the plurality of linked-list data structures is simply an alternative arrangement of the art."

The Examiner has further argued that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to modify Harriman et al.'687's system to incorporate that the packet controller is configured to provide each of the plurality of first type packet pointers to a selected one of the plurality of linked-list data structures." In addition, the Examiner has argued that "[t]he motivation to combine these teachings is to increase the replication rate of a switching fabric circuit having a multicasting capability that requires minimal buffer capacity for multicast connection traffic (column 1, lines 60-64)."

Applicant respectfully disagrees and asserts that, in Col. 1, lines 60-64, Harriman merely teaches that "[t]he invention is directed to a mechanism for increasing the replication rate of a switching fabric circuit having a multicasting capability that requires minimal buffer capacity for multicast connection traffic."

However, merely disclosing "a mechanism for increasing the replication rate of a switching fabric circuit having multicasting capability that requires minimal buffer capacity for multicast connection traffic" (emphasis added), as in Harriman, does not even suggest "provid[ing]...each of the plurality of first type packet pointers to a selected one of the plurality of linked-list data structures" (emphasis added), as claimed by applicant (see this or similar, but not necessarily identical language in the independent claims).

Because Harriman fails to teach or suggest "provid[ing]...each of the plurality of first type packet pointers to a selected one of the plurality of linked-list data structures" (emphasis added), as claimed by applicant, it cannot be said that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to modify Harriman et al.'687's system to incorporate that the packet controller is configured to provide each of the plurality of first type packet pointers to a selected one of the plurality of linked-list data structures," as argued by the Examiner. Applicant thus formally requests a specific showing of the subject matter in ALL of the claims in any future action.

With respect to dependent Claim 14, the Examiner has relied on Col. 11, lines 14-15; Col. 11, lines 18-20; and Col. 14, lines 60-61 from Raza to make a prior art showing of applicant's claimed technique "wherein...the plurality of status flags includes: a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication."

Applicant respectfully asserts that the excerpts from the Raza reference relied upon by the Examiner simply teach that "[t]he address generator circuit 402 may receive a signal (e.g., UNICAST_HTPR) from the logic block 404" (Col. 11, lines 14-15). Further, the excerpts teach that "[t]he signal UNICAST_HPTR may indicate a head pointer for unicast packets" and that "[t]he signal MULTICAST_HPTR may indicate a head pointer for multicast packets" (Col. 11, lines 18-20).

However, simply disclosing that "[t]he address generator circuit 402 may receive a signal (e.g., UNICAST_HTPR) from the logic block 404" where "[t]he signal UNICAST_HPTR may indicate a head pointer for unicast packets" (emphasis added), as in Raza, simply fails to teach "the plurality of status flags includes...a first type packet pointer head position indication" or "an overall head pointer indication" (emphasis added), as claimed by applicant.

Furthermore, in Col. 14, lines 59-62, Raza merely teaches that "[t]he registers 508a-508n may be configured to store information such as the head pointer address, the tail pointer address, the depth of each queue and/or the length of each queue." However,

simply teaching that "[t]he registers 508a-508n may be configured to store information such as...the tail pointer address" (emphasis added), as in Raza, simply fails to teach "a first type packet pointer tail position indication" (emphasis added), as claimed by applicant. Clearly, a "tail pointer address" (emphasis added), as in Raza, simply fails to teach a "packet pointer tail position indication" (emphasis added), as claimed by applicant.

Additionally, the Examiner has stated that "neither Harriman et al.'687 nor Raza et al.'349 teaches an overall tail pointer indication" but argues that "said over tail pointer indication is simply an alternative arrangement in the art" and "[i]t would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman et al. '687's system to incorporate, as taught by Raza et al. '349, that the plurality of status flags includes a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication." The Examiner further argues that "[t]he motivation to combine these teachings is to enable an apparatus to extract in-band information or skip extraction and perform a look ahead operation (column 3, lines 13-17)."

Applicant respectfully disagrees and asserts that in Col. 3, lines 13-17, Raza merely teaches that "[a]nother aspect of the present invention concerns an apparatus configured to extract in-band information or skip extraction of the in-band information and perform a look ahead operation" where "[t]he apparatus may be configured to switch between the extraction and the skipping of the extraction" (emphasis added). However, simply disclosing "switch[ing] between the extraction and the skipping of the extraction" (emphasis added), as in Raza, fails to even suggest "an overall tail pointer indication," as claimed by applicant. Accordingly, it cannot be said that "[i]t would have been obvious to one of ordinary skill in the art at the time of invention to modify Harriman et al. '687's system to incorporate, as taught by Raza et al. '349, that the plurality of status flags includes a first type packet pointer head position indication; a first type packet pointer tail position indication; an overall head pointer indication; and an overall tail pointer indication," as argued by the Examiner. Applicant thus formally requests a specific showing of the subject matter in ALL of the claims in any future action.

With respect to dependent Claim 20, the Examiner has relied on Col. 15, lines 58-60 from Raza to make a prior art showing of applicant's claimed technique "wherein...the first data structure is accessed at most once; and the second data structure is accessed at most once."

Applicant respectfully asserts that, in Col. 15, lines 58-60, Raza merely teaches that "the system 600 may allow each pointer to be written whenever a location is accessed (e.g., every eight cycles)." However, simply teaching that "the system 600 may allow each pointer to be written whenever a location is accessed" (emphasis added), as in Raza, simply fails to suggest applicant's claimed technique "wherein...the first data structure is accessed at most once; and the second data structure is accessed at most once" (emphasis added).

Again, applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above.

Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Still yet, applicant brings to the Examiner's attention the subject matter of new Claims 32-33 below, which are added for full consideration:

> "wherein: the port transmit controller is coupled to an output port" (see Claim 32); and
>
> "wherein: each of the plurality of FIFO structures are coupled with a corresponding set of output port status flags" (see Claim 33).

Again, a notice of allowance or a proper prior art showing of all of applicant's claim limitations, in combination with the remaining claim elements, is respectfully requested.

Thus, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. RMI1P041).

Respectfully submitted,
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